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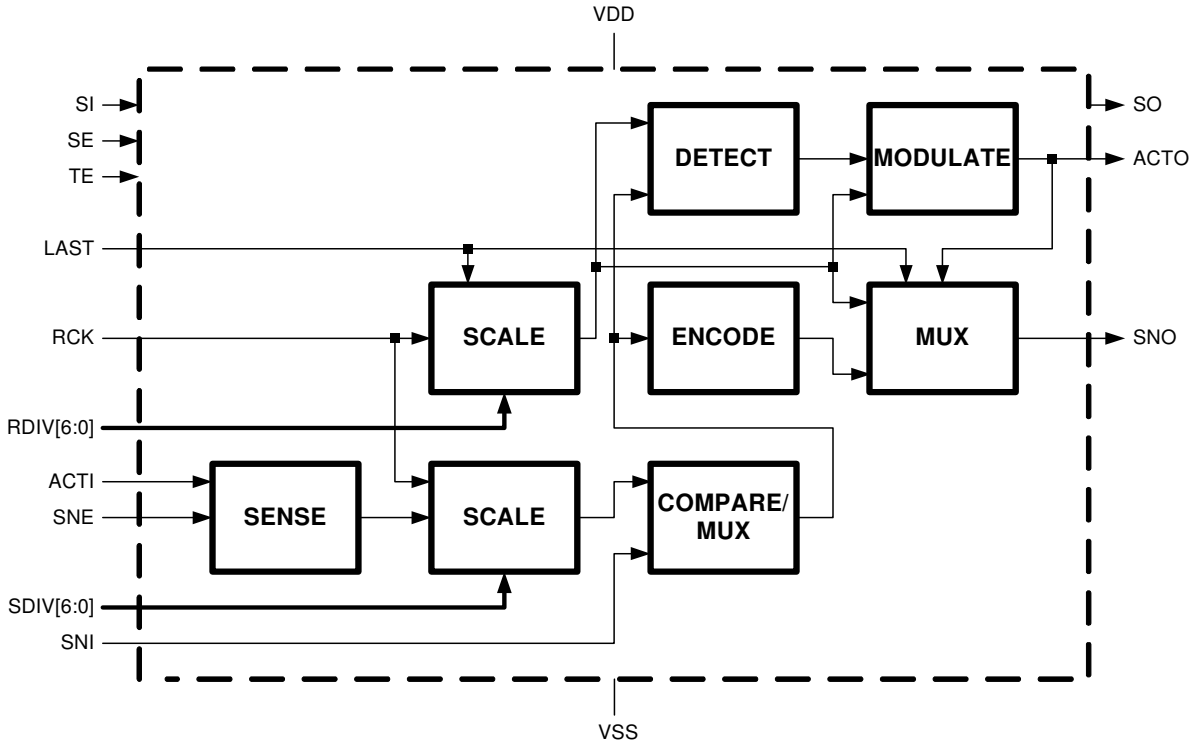
ACCEL™ Sensor S002 Data Sheet

Features

- Embedded sensor detects instantaneous operating parameters of load device
- Use with VR2002/2001 Accel regulator family to enhance ASIC/FPGA performance (achieve 35-45% speed/power improvement)
- "Black box" functionality has minimal impact on netlist connectivity
- Occupies minimal area (8100 um^2 in 90nm) in device layout
- Single pin interface to Accel regulator
- Low frequency, digital output signal
- Configurable for user-selectable performance control
- Available for ASIC and FPGA technologies below 180nm

Functional Block Diagram



(Rev 0.1)

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Description

The Accel™ Technology consists of a closed-loop voltage regulating system that directly controls the speed/power performance of the load device. It consists of two primary functions: (a) an embedded sensor which resides in the load device, and (b) an external regulator which controls the supply voltage of the load device. The sensor communicates with the regulator in closed-loop fashion to maintain a targeted performance level. The performance level is selectable by the user to optimize for maximum speed, minimum power, or some combination of each. This data sheet describes the Accel sensor, S002. It is intended to be used with the VR2002/2001 Accel regulator family. The Accel regulators are described in separate data sheets.

The Accel S002 sensor is a small IP block that detects instantaneous operating parameters of the load device. It communicates with the Accel regulator via a single pin interface. The sensor output is a low frequency digital signal that is compatible with generic I/O library pads.

Basic functional pins consist of an enable control input (SNE), a reference clock input (RCK), a modulation control interface (ACTO/ACTI) and a sense output (SNO). Additional pins are included for configuration purposes, interfacing multiple sensors, and scan test support.

The sensor should be physically placed in the layout of the load device such that it sees a representative voltage on the internal power supply distribution controlled by the Accel regulator. Multiple sensors can be connected together in daisy-chain fashion (using the SNI and SNO pins) where sensing of multiple blocks is required. See the pin connection diagrams for appropriate connectivity of single and multiple sensor configurations.

The sensor is enabled by a high level on the SNE input. When SNE is low, the sensor is completely disabled and in a low-current (< 1uA) shutdown state. A stable clock is required as a reference for detection of operating conditions and for internal timing control. The clock signal is applied to the RCK input and must be within a frequency range of 10 to 100MHz. For multiple sensors, a reference clock is only needed for the last instance. A modulation control interface is provided via the ACTO and ACTI pins to allow timing control of multiple sensors from the last instance. The LAST pin is used to designate the last instance in a chain of multiple sensors.

The S002 sensor can be configured via two 7-bit control words applied to the RDIV and SDIV inputs. These inputs control dividers for scaling the frequency of the reference clock and internal sense signals. The configuration values determine the target operating point for the load device.

A scan interface is provided to test the IP block. Dedicated pins for test enable (TE), scan enable (SE), scan data in (SI), and scan data out (SO) are provided. A test clock can be applied to the RCK input when test mode is enabled by a high level on the TE input. The analog sense block portion of the sensor can be tested by controlling the SNE and LAST pins to route the internal sense signal to SNO. For multiple sensors, each sensor can be tested individually by measuring the corresponding output signal at the ASIC/FPGA pin.

For applications that must be compatible with both the VR2001 and 2002 regulators, then a reference clock of the same frequency must be supplied to both the sensor and the VR2001 regulator.

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Pin Description

Name	Type	Description
Functional Pins		
ACTI	Input	Active in; modulation control input
ACTO	Output	Active out; modulation control output
LAST	Input	Last indicator; identifies last instance of multiple sensor chain
RCK	Input	Reference clock; also used for test clock
SNE	Input	Sense enable
SNI	Input	Sense in; for use with multiple sensors
SNO	Output	Sense out
Test Pins		
SI	Input	Scan data in
SE	Input	Scan enable
SO	Output	Scan data out
TE	Input	Test enable
Configuration Pins		
RDIV[6:0]	Input	Reference frequency control word
SDIV[6:0]	Input	Sensor frequency control word
Power Pins		
VDD	Power	Positive supply
VSS	Ground	Negative supply

Notes:

1) Bus notation for configuration pins are expanded to individual bits in Verilog model (RDIV_6 to RDIV_0 and SDIV_6 to SDIV_0).

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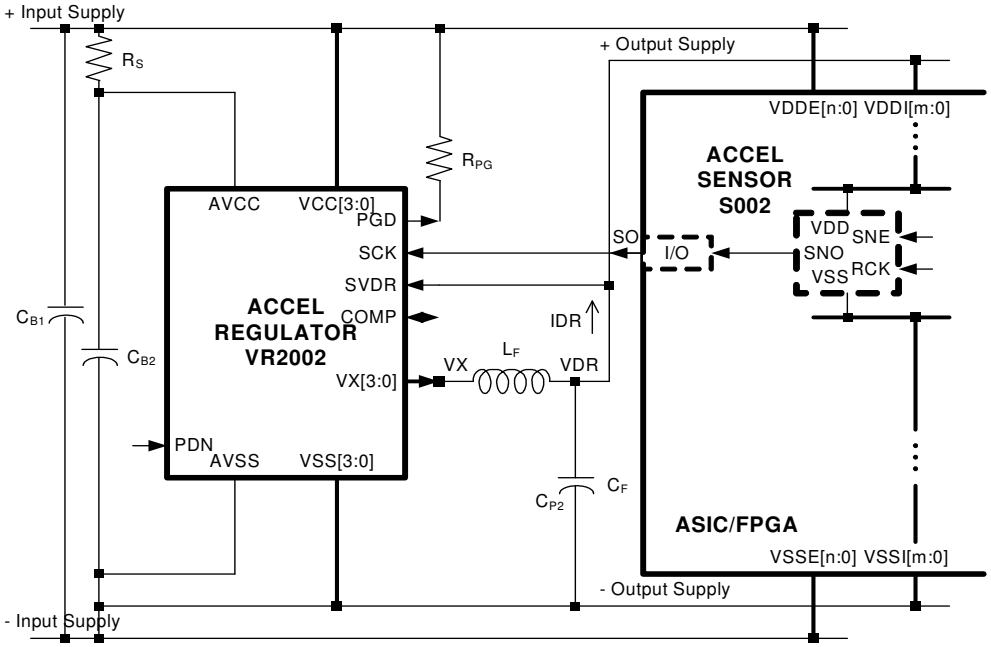
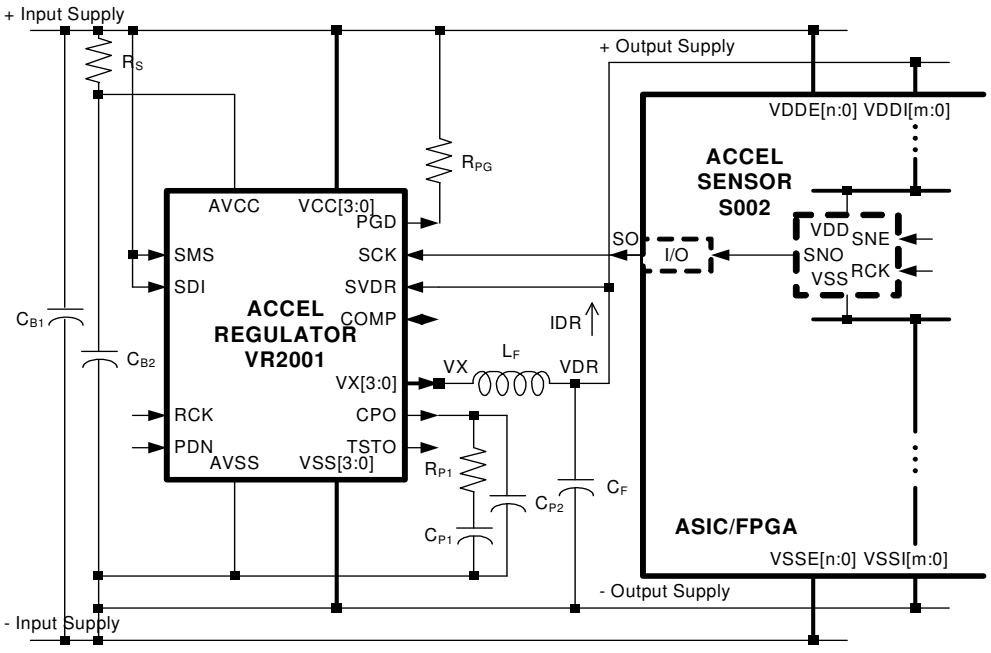
Typical Application Diagrams



(Rev 0.7b)

With VR2002 Regulator



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With VR2001 Regulator

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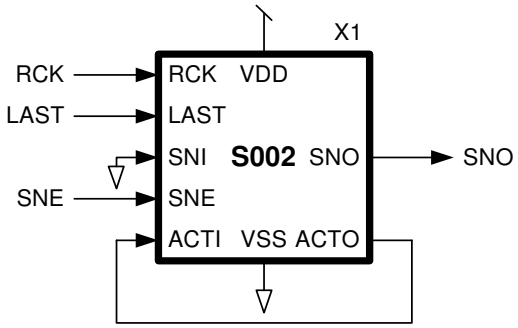
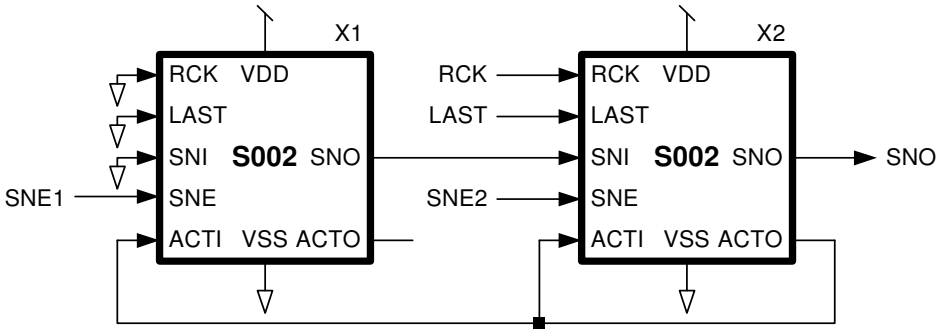
Pin Connection Diagrams

(Functional Pins Only)



Single sensor



Multiple sensors

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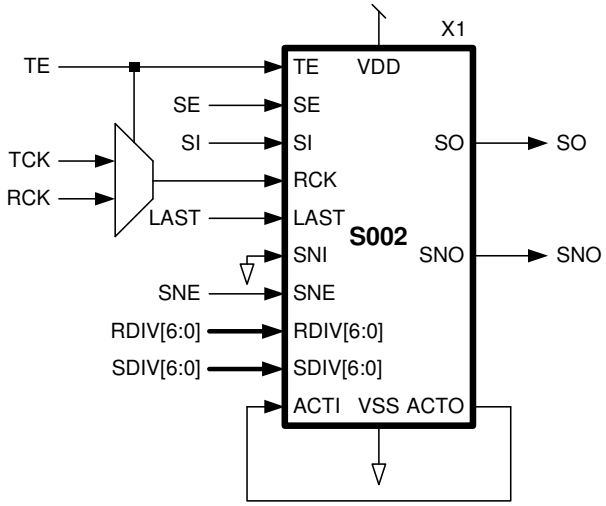
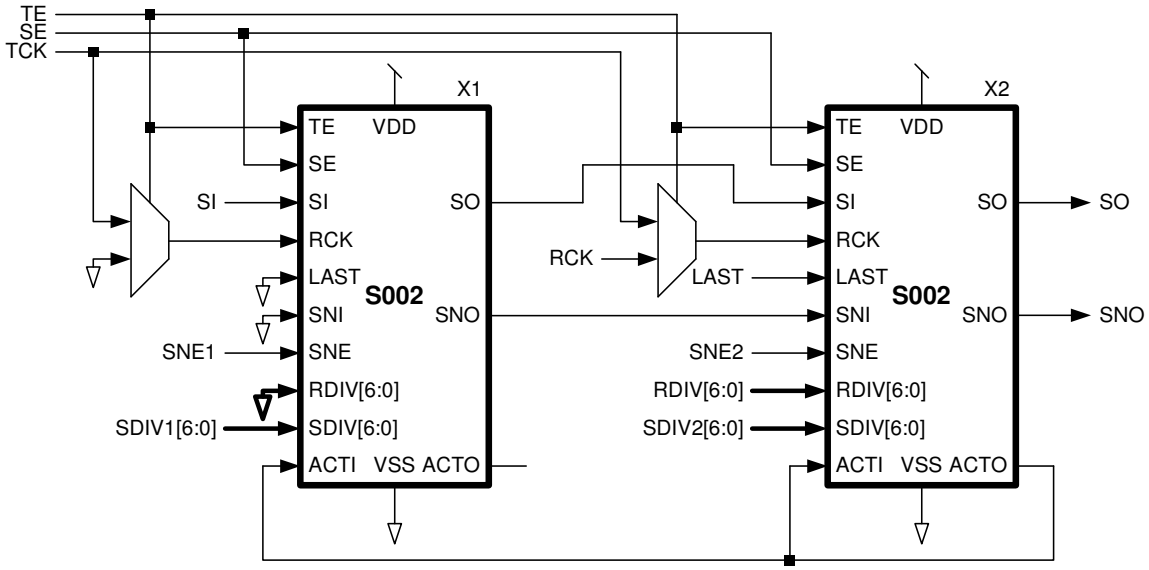
Pin Connection Diagrams

(Functional & Test Pins)



Single sensor



Multiple sensors

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Pin Configuration Tables

Single Sensor

Mode	Inputs												
										with VR2001		with VR2002	
	TE	SE	SI	TCK		SNE		SDIV	RDIV	RCK	LAST	RCK	LAST
Normal	0	0	X	X		1		<sn>	<ref>	0	0	RCK	1
Scan Test	1	SE	SI	TCK		SNE		SDIV	RDIV	X	LAST	X	LAST
Functional Test	0	0	X	X		1		<sn>	X	0	0	0	0

<sn> = sense target value
<ref> = reference target value

Multiple Sensors

Mode	Inputs												
										with VR2001		with VR2002	
	TE	SE	SI	TCK	SNE1	SNE2	SDIV1	SDIV2	RDIV	RCK	LAST	RCK	LAST
Normal	0	0	X	X	1	1	<sn1>	<sn2>	<ref>	0	0	RCK	1
Scan Test	1	SE	SI	TCK	SNE1	SNE2	SDIV1	SDIV2	RDIV	X	LAST	X	LAST
Functional Test 1	0	0	X	X	1	0	<sn1>	<sn2>	X	0	0	0	0
Functional Test 2	0	0	X	X	0	1	<sn1>	<sn2>	X	0	0	0	0

<sn1> = sense1 target value
<sn2> = sense2 target value
<ref> = reference target value

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Electrical Parameters

T_j = 0 to 125°C, VDD = Vnom +/-10% (technology dependent), VSS = 0V

Parameter	Description	Value			Units
		Min	Typ	Max	
f_{RCK}	RCK input frequency	10		100	MHz
f_{SNO}	SNO output frequency	1	2	5	MHz
t_{EN}	Sense enable time (SNE=1 to SNO valid)		1		us
t_{DIS}	Sense disable time (SNE=0 to SNO invalid)		1		us
t_{SU}	Set-up time (SE, TE to RCK _/)		2		ns
	Set-up time (SI to RCK _/)		100		ps
t_H	Hold time (SE, TE to RCK _/)		200		ps
	Hold time (SI to RCK _/)		100		ps
t_{PLH}/t_{PHL}	Prop delay time (RCK _/ to SO, C_{SO}=0pF)		400		ps
IDD	Average operating current (SNE=1, C_{SNO}=0pF)		200		uA
IDDq	Quiescent supply current (SNE=0)		1		uA