iSine
FABLESS SEMICONDUCTOR SOLUTIONS

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Die Size Estimate in 3 technologies: 0.18um, 0.35um, 0.6um CMOS

Small mixed signal design example: balanced analog and digital content

Estimated production volume: 1,000,000 units/year

	Description	0.18um, 8" wafer 1P4M, HIRES poly Source	Area (um^2)	0.35um, 8" wafer 1P4M, HIRES poly Source	Area (um^2)	0.6um, 8" wafer 1P4M, HIRES poly Source	Area (um^2)
Analog & OTP:							
	Bias and BGR	int. IP	95,400	int. IP	114,480	int. IP	137,376
	POR	int. IP	16,200	int. IP	19,440	int. IP	23,328
	Lin reg & soft-start	custom	70,000	custom	84,000	custom	100,800
	Xtal osc circuit	I/O lib	20,000	I/O lib	24,000	I/O lib	28,800
	10.4s+ timer	custom	210,000	custom	252,000	custom	302,400
	temp sense blk	custom	40,000	custom	48,000	custom	57,600
	8b ADC	IP	90,000	custom	108,000	custom	129,600
	10b DAC	custom	35,570	custom	51,110	custom	167,534
	PLL	IP	132,000	IP	158,400	IP	190,080
	power amplifier	custom	80,000	custom	96,000	custom	115,200
	DAC-based mixer	custom	30,000	custom	36,000	custom	43,200
	OTP 32 x 1	IP	56,448	IP	67,738	IP	81,285
		Analog area:	**875,618**	Analog area:	**1,059,168**	Analog area:	**1,377,204**
Digital:							
	logic gates	60,000		logic gates	60,000	logic gates	60,000
	density	(gates/mm^2)	100,000	density	(gates/mm^2)	25,000	density (gates/mm^2)	7,500
		Digital area:	**600,000**		Digital area:	**2,400,000**	Digital area:	**8,000,000**
Pads:		std H (um) 257	std W (um) 60	std H (um) 424	std W (um) 100	std H (um) 430	std W (um) 110
1	XTAL osc (1MHz)	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
2	"	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
3	VDD	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
4	VBATT	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
5	VSS	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
6	RF+	custom	15,420	custom	42,400	custom	47,300
7	RF-	custom	15,420	custom	42,400	custom	47,300
8	Program V	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
9	EnableA	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
10	EnableB	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
11	test	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
12	Vreg	I/O lib	15,420	I/O lib	42,400	I/O lib	47,300
12-24	various	I/O lib	185,040	I/O lib	508,800	I/O lib	567,600
		Pad cell area:	**370,080**	Pad cell area:	**1,017,600**	Pad cell area:	**1,135,200**
DIE SIZE TOTALS:							
		analog	875,618 um^2	analog	1,059,168 um^2	analog	1,377,204 um^2
		digital	600,000 um^2	digital	2,400,000 um^2	digital	8,000,000 um^2
		pads	370,080 um^2	pads	1,017,600 um^2	pads	1,135,200 um^2
			1,845,698 um^2		4,476,768 um^2		10,512,404 um^2
		routing/margin multiplier:	1.3	routing/margin multiplier:	1.3	routing/margin multiplier:	1.3
			2,399,407 um^2		5,819,798 um^2		13,666,125 um^2
		Xdimension	1.72 mm	Xdimension	2.20 mm	Xdimension	2.32 mm
		Ydimension	1.40 mm	Ydimension	2.65 mm	Ydimension	5.89 mm
		yield (GDW)	10,600	yield (GDW)	4,500	yield (GDW)	1,900
		# wafers/year	*94*	# wafers/year	222	# wafers/year	526
		**** too few wafers/year for fab minimum requirement****		**BEST CHOICE**			
		relative die cost:	-	relative die cost:	0.56	relative die cost:	1.00
	NRE costs ammortized over 2 year's production including engineering costs, masks, wafers, & test (per die):				$0.20		$0.19